REMARKS

Applicants further respond to the Examiner's detailed October 5, 2005 Office Action with the following remarks organized according to the Examiner's communication. In addition, minor amendments have been made to certain claims. No new matter has been added by any of these minor changes.

In the Office Action mailed October 5, 2005, claims 1, 3, and 4 were rejected under 35 U.S.C. § 103 (a) based upon a combination of U.S. Patent No. 6,798,044 (Joshi) and a published U.S. application U.S. 2002/0113305 (Huang). Claim 2 was rejected based upon those two combined with U.S. 2003/089248 (Estacio). Claims 5, 6, and 9 – 15 were rejected based upon those two combined with U.S. 6,476,481 (Woodworth et al).

Responsive to the Examiner's rejection of Claims 1, 3, and 4 under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Huang, Applicant respectfully requests reconsideration in light of the current amendment. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The present invention is neither taught nor suggested by Joshi combined with Huang.

Joshi teaches **one** technique – flip chip mounting – for connecting two dies to a lead frame. Specifically, Joshi provides "a chip device that includes two dies stacked atop one another. The use of solder bumps allows for a small package profile," column 1, lines 42 - 44. Joshi does not teach using different mounting connections for each die. Nor does Joshi teach connecting a die via wire bonding.

In contrast, Independent Claim 1 of the present invention includes the limitation of "an integrated circuit mounted on the upper surface of the die pad and **having contact areas for receiving bond wires; bond wires extending from the contact areas on the integrated circuit to the outer leads of the leadframe**; one or more power mosfet semiconductor devices flip chip mounted on the lower surface of the leadframe." The claims are distinctive from Joshi because the language "having contact areas for receiving bond wires" indicates that each of the two dies are mounted using **different** techniques, while Joshi teaches only **one** technique for mounting **both** dies.

The present claims are directed to an invention that has the advantage of being a multi-chip package with flip chip features and a wire bonded fully encapsulated device, whereas Joshi is limited to flip chip mounted device, as stated by Joshi in lines 9 and 10 of column 3. As a result, Joshi requires that surfaces be exposed on both dies on both sides of the package. Huang, teaching a fully encapsulated package wherein both dies are wire bonded, does not overcome these deficiencies. Wire bonded dies are fully encapsulated, have no exposed surface, and - prior to the present invention - were considered incompatible with flip chip packaging.

A prima facie case of obviousness may be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Joshi explicitly teaches away from wire bonding as a method for attaching the dies. Joshi states, "**the non-use of wire bond interconnect** allows for accommodating a very large size die for a given molded package body outline," column 1, lines 44 – 49 (emphasis added), and "**the non-use of wire bond interconnect** allows for accommodating a very large size die for a given molded package," column 3, lines 9 – 11 (emphasis added). In contrast, Claim 1 of the present invention explicitly employs a wire bonding technique as discussed above.

Like Joshi, Huang also teaches away from the present invention. Specifically, Huang teaches away from: (1) flip chip mounting; and (2) mounting both dies on a **single** lead frame using a **single** die pad. Huang requires two lead frames, each with its own die pad. Huang claims "a first leadframe having a die pad...a second leadframe having a die pad..." paragraphs [0047] – [0048]. The use of two lead frames and two die pads is central to Huang's invention. He suggests that flip-chip mounting two dies to only one

lead frame and one die pad may result in the two dies becoming "damaged," "imprecisely aligned," "deformed," or "delaminated," paragraphs [0016] – [0022]. In contrast, Independent Claim 1 of the present invention is directed toward "one lead frame," and is limited to a single lead frame and a single die pad.

There is no suggestion to combine Joshi and Huang. If one followed Huang and combined Huang and Joshi, one would use **two** die pads and **two** lead frames. Moreover, one skilled in the art would be led to selecting **either** wire bonding or flip chip mounting for **both** dies, as Joshi teaches away from wire bonding and Huang teaches away from flip-chip mounting. The Examiner has not pointed out any suggestion in Joshi or Huang to combine both wire bonding and flip chip mounting on a single dual-die device. There is no disclosure in either reference to mix connection types.

Responsive to the Examiner's rejection of Claim 2 under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Huang and Estacio, Applicant respectfully requests reconsideration in light of the current amendment. The Examiner correctly points out neither Joshi nor Huang recite source bump contacts in the surface of the MOSFETs and the gate bump contacts extending to a corresponding outer lead. As discussed above, there is no suggestion to combine Joshi with Huang. In addition, there is no suggestion to combine these references with Estacio to overcome these deficiencies.

Joshi and Huang are directed toward dual-die stacked devices. Estacio is directed toward a method for creating "dual or multiple gate pads for a single gate contact" on a single MOSFET die, paragraph [0018]. Particularly, Estacio is directed toward a method for extending "under-bump metal laterally from the gate contact with the gate pad metallization out to two or more gate pads not overlying the gate pad metallization," paragraph [0007] (emphasis added). Joshi teaches a "single, common lead frame," and a first and second "bumped die" flipped and soldered to the lead frame, column 3, lines 17 - 25. Joshi does not teach source bump contacts in the surface of the MOSFETs, and the gate bump contacts extending to a corresponding outer lead. Huang teaches a dual-die integrated circuit package employing a wire bond process. The Examiner has failed to point out a suggestion in Estacio to combine his invention with one that employs wire bond interconnects, or one for creating a dual-die stacked device incorporating multiple connection types.

Responsive to the Examiner's rejection of Claims 5, 6, and 9 - 15 under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Huang and Woodworth, Applicant respectfully requests reconsideration in light of the present amendment. The Examiner correctly points out Joshi does not suggest the following elements found in the present invention: (1) source bump contacts in the surface of the MOSFETs and gate bump contacts extending to a corresponding outer lead; (2) die pad terminology; (3) bonding wires; nor (4) different connections from ball grid or stud grid. Huang does not suggest using a single lead frame and die pad nor flip chip mounting. It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). As discussed above, Joshi explicitly teaches away from wire bonding connections. Similarly, Huang explicitly teaches away from flip-chip mounting, as well as the use of a single lead frame and a single die pad. These elements are also found in the present invention.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). The Examiner has pointed out no suggestion to combine these references with Woodworth to overcome these deficiencies.

Woodworth teaches a semiconductor with a single die, a plurality of bonding wires, a die mounting pad, and a plurality of external conductors reentrantly bent and penetrating a side wall of a plastic housing (column 7, lines 1-17). Woodworth does not teach a dual-die structure, nor a dual-die structure with a ball array or stud array connection.

Applicant respectfully submits that Claims 5, 6, and 9 - 15 are therefore in condition for allowance.

Applicants anticipate that an interview may be necessary to address matters that may put the foregoing claims in condition for allowance in light of the recent amendments. The Examiner is invited to call the undersigned attorney to facilitate allowance of the application.

Applicants respectfully request favorable consideration and that a timely Notice of Allowance be issued in this case.

In the event that Applicant has overlooked the need for an extension of time, additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefore and authorize that any changes be made to Deposit Account No.: 50-3010.

Respectfully submitted,

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